Jump Start in Verification Using Specman Elite

Productive Knowledge Series in Verification

This printed brochure gives an overview of what is covered in each section of the course, identifies the prerequisites, and offers contact information. This content is designed to work with a more general brochure that presents the benefits of attending a Qualis course, and the web site that presents a more detailed syllabus, lists the schedule, and offers online registration. Drafted, edited, and formatted this brochure. Qualis (www.qualis.com) is a verification IP, consulting, and training firm.

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Course overview

This three-day interactive course teaches you the basics of the *e* language, the Specman Elite™ environment and the basic skills you need to implement testbenches for complex ASIC, FPGA and board-level designs. The course is rich in methodology hints and tricks used by our verification experts who regularly verify 5+ million gate systems. With the help and guidance of our experienced verification consultants, you will learn:

- The introduction to *e* and Specman Elite presents the tool, its interfaces, and its language. This section explains why you would use Specman Elite over an HDL and describes the relationship between Specman Elite and your simulator. You see how to invoke the tool and use the GUI. This section also gives you a jump start on the most basic commands.
- *e* The Language describes structs, units and methods, and working with data packets.
- *e* The Language Actions details the syntax and structure of the language in a familiar single-thread, sequential environment similar to C or PERL. This section also introduces an important feature, unique to Specman Elite, that allows existing code to be user-extended without modification. In addition to learning how to extend structs, methods, and types, you'll learn about language actions.
- The "*spec*" in Specman Elite comes from the ability to generate data values and sequences that follow a set of constraints. This section presents how your design specification is turned into a set of constraints. Lists are introduced for the generation of sequences and physical fields are used to map high-level data types to bit-level data streams. The basic concepts of automatic random data generation, object-oriented data representation and inheritance are also presented.
- The notion of time in Specman Elite is introduced with the concept of events. Events, coupled with temporal expressions and time-consuming methods, can express the most complex time-based relationships and bus-functional models.
- Verifying your design involves interfacing your Specman Elite testbench with your Verilog or VHDL model. This section presents how to access signals in the HDL simulation and how X's and Z's are handled. Events and expects are used for verifying the temporal dimension of your design's response.
- Functional coverage is an important concept that is well supported by Specman Elite. Just as code coverage is used to measure how well a testsuite executes the code of your design, functional coverage is used to measure how thoroughly a testsuite exercises your design.

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- Methodology guidelines identifies key guidelines and steps through a complete example to illustrate making the best use of Specman Elite.
- Miscellaneous utilities introduces you to the built-in productivity-enhancing features of Specman Elite and how to best implement a verificationenvironment with it.

Who should attend

If you need to verify a design with a high-degree of confidence, implement it testbenches, and have no or very little prior knowledge of the fundamentals of *e* or Specman Elite, then this course is for you.

The learning environment

This is an interactive course with numerous labs that cement the concepts taught in the lecture portion of each session. Students will use the latest version of Specman Elite.

This class can be taught using either Verilog or VHDL as the design language. Be sure you sign-up for or request a class that uses the HDL you prefer.

How to attend this course

You can attend a regularly scheduled public course, or schedule your own private session at your facility.

To see our schedule of public courses and to register online, visit our website at: www.qualis.com.

Schedule a private course at your facility when you have many people who wish to attend. Private courses can be customized to meet your specific needs. To contact us about a private session:

- In North America contact Nancy Hur at nancy@qualis.com or 1.503.968.8540.
- In Europe and Israel contact Andrew Betts at andrew.betts@qualis.com or +33 (0) 4.76.61.88.56.

About our other courses

From synthesis to verification to design reuse, our tightly-focused courses deliver the critical knowledge you need for ASIC, system and reusable IP design. We distill the best-of-the-best design techniques and know-how into multi-day courses, so you learn more of the latest proven methods in HDL/HVL-based design. Here's a sampling of the courses we offer:

Verification Methodology Using Specman Elite

- Jump Start for Verification - 3 days
- Deep Knowledge in Verification - 5 days
- Expert Verification Strategies - 2 days

Verification Methodology Using Verilog and VHDL

- Jump Start for Verification - 3 days
- Deep Knowledge in Verification - 5 days
- Expert Verification Strategies - 3 days

Synthesis Methodology Using Verilog and VHDL

- Jump Start for Synthesis - 3 days
- Deep Knowledge in Synthesis - 5 days
- Expert Synthesis Strategies - 3 days

System Design Methodology Using Verilog and VHDL

- High Level Design Using VHDL - 5 days
- High Level Design Using Verilog - 5 days

Design Reuse

- Designing with Reuse in Mind - 3 days
- Making Reuse Happen - 1 day

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